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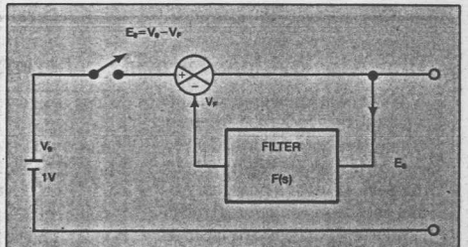
Basic program eases analysis of phase-locked loops

Analyzing second- and third-order phase-locked loops yourself can be a tedious and time-consuming task. Using a Basic program, you can employ a small computer to perform all the necessary tasks much faster.

Ron Rippy, *Durham, NC*

Relying on a Basic program and a computer, you can model a third-order tracking filter (or phase-locked loop) with a linear phase detector and plot the error response E_0 to a phase step of 1 rad (**Ref 1**). A similar approach allows you to analyze PLLs (second- and third-order) with sine-wave phase detectors and compare the two types of loops. You can study the two loops' error response to frequency and acceleration steps as well as to high-level random noise and sine-wave inputs, all of which can drive a loop into the nonlinear phase region of the phase detector.

Fig 1 shows a block diagram of a phase-locked loop along with the Basic program that allows you to calculate and plot E_0 for a third-order loop. (For a detailed description of phase-locked loops, see **box**, "Phase-locked loops provide coherent tracking.") The second-order loop's phase response is expressed by the second-order equation in **Fig 1**. This loop is a high-gain type (**Ref 2**), whereas the third-order loop is a Wiener loop optimized for minimum phase error when the input is a frequency ramp.



THIRD-ORDER EQUATION:

$$E_o = -2\omega\frac{1}{s}E_0 - 2\omega^2\frac{1}{s^2}E_0 - \omega^3\frac{1}{s^3}E_0 + V_0$$

SECOND-ORDER EQUATION:

$$E_o = -2d\omega\frac{1}{s}E_0 - \omega^2\frac{1}{s^2}E_0 + V_0$$

WHERE
d=DAMPING FACTOR=0.707
ω=NATURAL FREQUENCY=1 RAD/SEC
s=LAPLACE OPERATOR

```
3000 E0,E1,E2,E3=0 @ V0,W=1
3010 SCALE 0,8,-.5,1.5
3020 XAXIS 0,1 @ YAXIS 0,.1
3030 MOVE 0,0 @ T=.05
3040 FOR X=0 TO 8 STEP T
3050 E1=T*E0+E1
3060 E2=T*E1+E2
3070 E3=T*E2+E3
3080 E0=-(2*W*E1)-2*W*W*E2-W*W*W*E3+V0
3090 DRAW X,E0
3100 NEXT X
3110 END
```

Fig 1—Depending on whether your PLL is a second- or third-order loop, phase response is expressed by either a second- or third-order equation. The Basic listing solves the third-order equation.

The second-order loop doesn't lock when subjected to a 1-rad/sec² acceleration step, its acceleration pull-out step size.

To change from a linear to a sine-wave phase detector, you simply replace E_0 on line 3050 of the program with $\sin(E_0)$. Thus, E_0 equals $\sin(V_0-V_F)$ rather than simply V_0-V_F, as shown in **Fig 1**. To change V_0 to an n rad/sec frequency step, or an n rad/sec² acceleration step, you enter n*X or n*X*X/2, respectively, for V_0 on line 3080. To change V_0 to an n radian peak sine wave, you enter n*SIN(W*X) in place of V_0.

Fig 2 illustrates the second- and third-order loops' error response to unity-phase, frequency, and acceleration steps. *(Ed Note: For all figures, the second- and third-order plots are shown as dashed and solid lines, respectively.)* Note that when the second-order loop is subjected to a 1-rad/sec² acceleration step (the acceleration pull-out (APO) step size), it doesn't lock. It will lock for a 0.9-rad/sec² acceleration step, but it will have approximately a 1.1-rad steady-state phase error. On the other hand, the third-order loop, with its additional integrator, is able to reduce the steady-state error to 0.

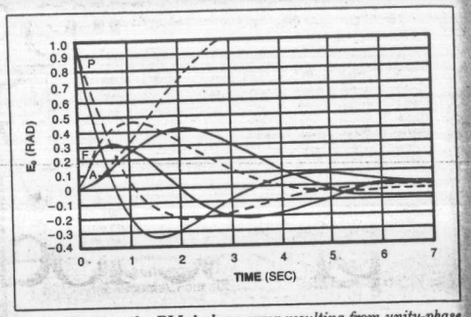


***Fig 2—Plotting the PLLs' phase error** resulting from unity-phase (P), frequency (F), and acceleration (A) steps shows that the third-order loop can track a unity acceleration step, but the second-order loop cannot.*

You'll find that as you try increasingly larger phase steps, both loops unlock at 3.2 rad, but remain in lock at 3.1 rad (**Fig 3**). Lock loss occurs at 3.2 rad (just over 3.14 rad, actually) because the sine-wave phase detector sends the wrong polarity voltage to the loop filter when the error exceeds π rad. The wrong polarity voltage causes the phase error to increase rather than decrease.

In **Fig 4**, ωPO (the frequency pull-out that causes loss of lock) occurs at 3.1 rad/sec in the second-order loop and 4.7 rad/sec in the third-order loop. The values correspond to a normalized loop frequency of 1 rad/sec. **Fig 5** shows that APO equals 1 rad/sec² for the second-order loop, and 3 rad/sec² for the third-order loop. JPO (the phase-jerk pull-out, or linearly increasing accelera-

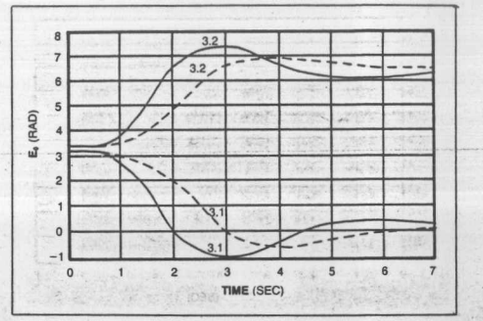


***Fig 3—Neither loop remains locked** for phase steps above 3.1 rad. The sine-wave detector forces both loops to relock at 2π rad—behavior referred to as cycle slipping.*

Phase-locked loops provide coherent tracking

A phase-locked loop, or PLL, is a circuit that locks the frequency of one oscillator to that of a second oscillator. In **Fig Aa**, the master oscillator's phase is V_0, and the slave voltage-controlled oscillator (VCO), which locks to and follows the frequency of V_0, has a phase of V_F.

The phase detector subtracts V_F from V_0 to produce a voltage E_0 that's proportional to the phase difference (error) between the two oscillators. After amplification and filtering, E_0 feeds back to the VCO, forcing a frequency change that reduces (or totally eliminates, in some loops) the phase error. To realize a lock condition, the steady-state frequency (but not the phase) error must be 0.

The loop filter prevents high-frequency noise and modulation on V_0 from reaching the VCO. This filtering ensures that the VCO will follow only slow changes in the frequency of V_0.

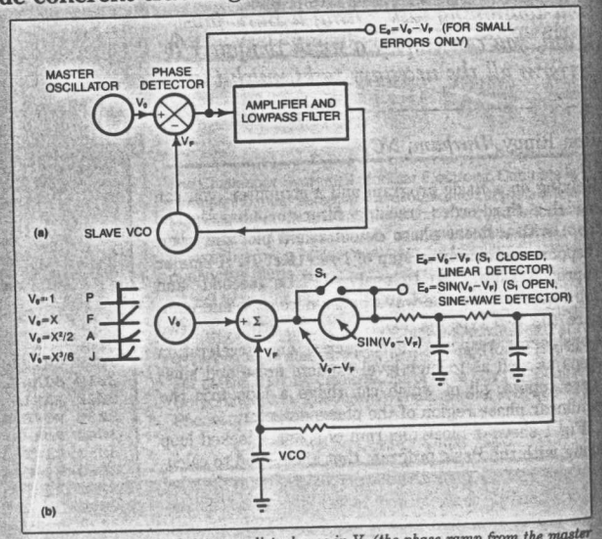


Fig A—In a basic PLL (a), any disturbance in V_0 (the phase ramp from the master oscillator) produces an error E_0, which forces V_F (the phase ramp from the slave oscillator) to match and cancel V_0. In the conceptual diagram (b), the loop behaves as if S_1 is closed for small (less than 1 rad) phase disturbances in V_0 and open for larger disturbances.

The phase detector provides an output proportional to $\sin(V_0-V_F)$. For small phase errors, $\sin(V_0-V_F)\approx V_0-V_F$, and the output is linearly proportional to the phase error. For large errors like those that occur when the loop is about to lose lock, however, the output traces a sine wave.

The error voltage peaks at $\pi/2$; it then decreases even though the error continues to increase. This behavior is a result of the slope reversal of the sine wave above $\pi/2$ and is a source of instability in the loop. In fact, the loop may make the error larger rather than smaller.

The loop will not necessarily lose lock just because the error exceeds $\pi/2$. The shape and duration of the error waveform also come into play. For example, a phase step won't cause loss of lock until it exceeds π rad. Fortunately, once the error progresses a full 2π rad, the slope of the sine wave is again correct, and the loop may relock. The loop tendency to unlock and then relock in 2π rad is called cycle slipping.

Fig Ab separates the phase detector into linear and nonlinear components and shows the loop consisting of three integrators. The first two integrators following the detector constitute the filter, and the third integrator is the VCO. The VCO is a perfect integrator because a phase step in the oscillator causes a perpetual phase ramp (frequency step) in the output.

Assuming the loop is locked initially, both V_0 and V_F are identical steady-state phase ramps that cancel in the phase detector and leave no phase error. This quiescent condition poses no problem, of course. What is important is what happens to E_0 when a disturbance takes place in V_0. If two loops have identical bandwidth, the one that can withstand the greater disturbance and remain in lock is considered superior.

Fig A lists four disturbances—phase step (P), frequency step (F), acceleration step (A), and jerk step (J)—that are popular for testing loops. Each successive disturbance is an integral of the previous one, and you substitute each one for V_0 on line 3080 of the Basic program.

In general, a loop with only one integrator (the VCO) will track phase disturbances having first-order or lower curvature (such as P and F). A loop with two integrators will track disturbances having second-order or lower curvature (eg, P, F, and A). This tracking performance is only possible if the disturbance is slow enough to pass through the loop filter and has a duration that's short enough to prevent the phase excursions from saturating amplifiers or other components in the loop.

If an exact trajectory is important as a loop begins to lose lock, you should keep the sampling step size at 0.01 sec max.

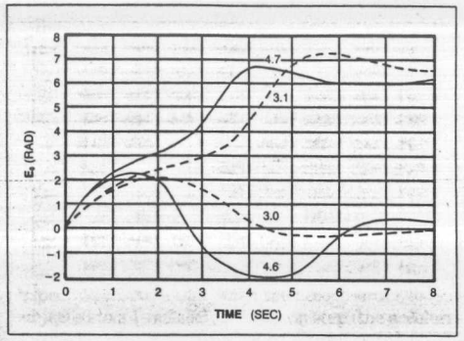


***Fig 4—Until cycle slipping begins,** the third-order loop can withstand a larger frequency step than the second-order loop.*

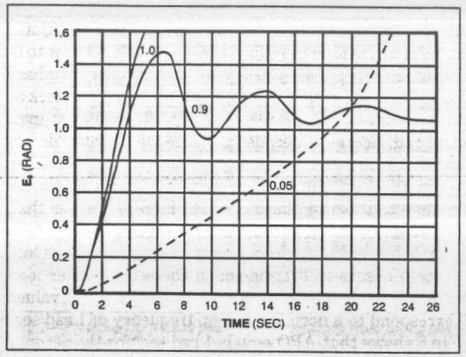


***Fig 6—The second-order loop is incapable of tracking** any finite value of jerk. The third-order loop will track a 0.9-rad/sec³ jerk step, but has a phase error of 1.1 rad.*

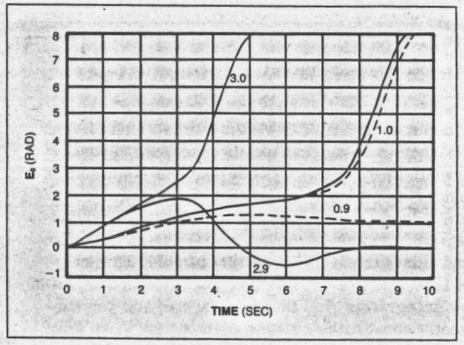


***Fig 5—The second-order loop can track an acceleration step** of 0.9 rad/sec², but has a 1.1-rad phase error. In contrast, the third-order loop can track a 2.9 rad/sec² step with a phase error of 0 rad.*

tion, that causes loss of lock) measures 1 rad/sec³ for the third-order loop, and less than 0.05 rad/sec³ for the second-order loop (**Fig 6**). Evidently, the second-order loop won't remain locked for any finite value of jerk input.

As far as accuracy is concerned, the sampling interval for the numerical integration process (T on line 3030 of the program) is 0.05 sec. If you reduce this interval to 0.01 sec, you'll wind up with the solid curve beside the 1 rad/sec² dashed curve in **Fig 5**. Reducing the interval even further (to 0.005 sec, for example) fails to change the curve—there's no noticeable improvement in accuracy.

At a 0.05-sec sampling rate, the error is low where the curves have a small or moderate slope, but it increases (to 0.5 rad or more) in regions where the curves have a steep slope. If it's important to have an exact trajectory as a loop begins to lose lock, then you should use a sampling step size no larger than 0.01 sec.

The set of curves in **Fig 7** reflects the third-order loop's performance for a series of acceleration steps in the 2.9- to 3.04-rad/sec² range—just above and below the value that'll lead to lock loss. As the curves illustrate, the loop responds first by locking properly but then begins to slip cycles; it loses lock and then relocks in 6.28-rad increments.

To this point, the results seem to indicate that the third-order loop outperforms the second-order loop. At the very least, the third-order loop accommodates larger frequency and acceleration steps before it loses lock.

Nevertheless, it isn't apparent how the two loops compare when noise is present. Fortunately, you can set up a comparison easily. You just make V_0 a pseudo-random waveform that varies from −3 to +3 rad p-p, an input that makes E_0 very noisy. You then make a plot of V_F, thereby taking advantage of the loop filter's quieting effect. The loop noise bandwidth equals 0.530ω for the second-order loop and $\frac{5}{6}\omega$ for the third-order loop. To equalize the noise level in both loops, ω should equal 1 for the second-order loop and 0.636 for the third-order loop.

The test for both loops uses the same five seed values for the random-noise generator. **Fig 8** shows that the third-order loop loses lock five out of five times, where-

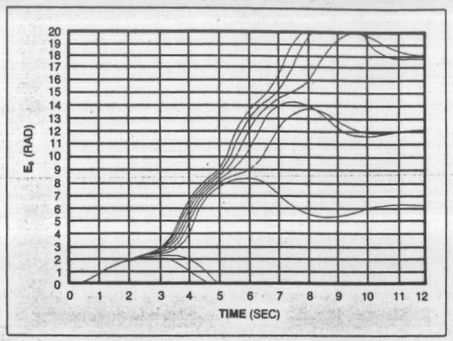


***Fig 7—Multiple cycle slips occur in the third-order loop** for acceleration steps above 3 rad/sec². The slope of each phase curve is equal to the frequency difference between the master and slave oscillators.*

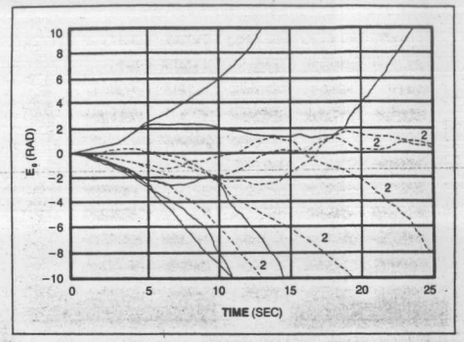


***Fig 8—At high noise levels,** the third-order loop tends to lose lock before the second-order loop.*

as the second-order loop loses lock just three out of five times. To make the performance of both loops virtually identical, you must reduce ω in the third-order loop to 0.509. This reduction yields a noise bandwidth of $\frac{5}{6}\cdot 0.509 = 0.424$ rad/sec. The third-order loop shows about a 1-dB degradation in noise performance for these conditions.

Comparing stability of both loops

It's important to compare the stability of both loops. The third-order loop has the potential for becoming unstable: It has one more integrator, and hence more loop phase shift than the second-order loop. If no software is available to make a Bode plot, you can use a large sine wave (at the loop's natural frequency) for V_0 as an experiment. **Fig 9** shows error-voltage test results when V_0 equals $1.5\cdot\sin(1\cdot X)$. As the curves illustrate, E_0 continuously increases in the third-order loop until it loses lock. It takes more than 2 rad to cause a lock loss in the second-order loop. This data indicates that the third-order loop is probably more unstable than the second-order loop.

Table 1 provides a summary of the results of the analyses. The third-order loop withstands larger frequency, acceleration, and jerk steps before losing lock. On the negative side, however, large sustained signals —such as sine waves and noise—cause the third-order loop to lose lock earlier than the second-order loop. The third-order loop's increased phase shift is probably a contributing factor.

However, you can't overlook the sine-wave detector as a problem source because no indication of instability exists when you model either loop with a linear phase detector. Unfortunately, once the phase-shift error exceeds $\pi/2$ rad, $\sin(E_0)$ begins to decrease as E_0 continues to increase. A smaller $\sin(E_0)$ will reduce the value of V_F. Since $E_0 = V_0 - V_F$, E_0 will continue to increase and further decrease the value of $\sin(E_0)$. Evidently, the sine-wave detector seems to cause positive feedback.

To illustrate this effect, **Fig 10a** plots various parameters in the second-order loop when $V_0 = 2.1\cdot\sin(1.0\cdot X)$. The arrow indicates approximately where the sequence of events noted above begins to take place. **Fig 10b** shows the same measurements for a second-order loop

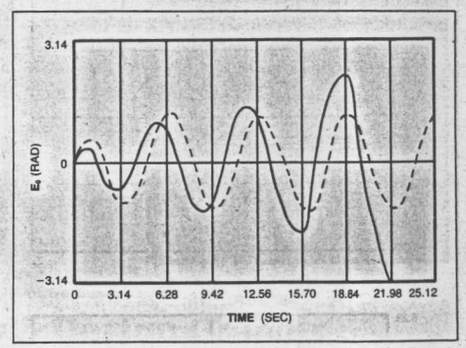


***Fig 9—The error voltage in the third-order loop** increases until lock is lost when V_0 is a 1.5-rad sine wave. Although the second-order loop looks stable, it loses lock when V_0 is increased to 2.1 rad.*

Results show that the third-order loop can withstand greater frequency and acceleration steps before losing lock.

TABLE 1—SUMMARY OF SECOND- VS THIRD-ORDER LOOPS WITH SINE-WAVE PHASE DETECTORS

TEST	SECOND ORDER	THIRD ORDER
PPO (RAD)	3.14	3.14
ωPO (RAD/SEC)	3.1	4.7
APO (RAD/SEC²)	1.0	3.0
JPO (RAD/SEC³)	>0	1.0
NOISE (3.0 RAD)	THIRD-ORDER LOOP LOSES LOCK BEFORE SECOND-ORDER LOOP. ABOUT 1-dB DIFFERENCE IN PERFORMANCE.	
SINE WAVE (1.5 RAD)	THIRD-ORDER LOOP LOSES LOCK. SECOND-ORDER LOOP LOSES LOCK AT 2.1 RAD.	

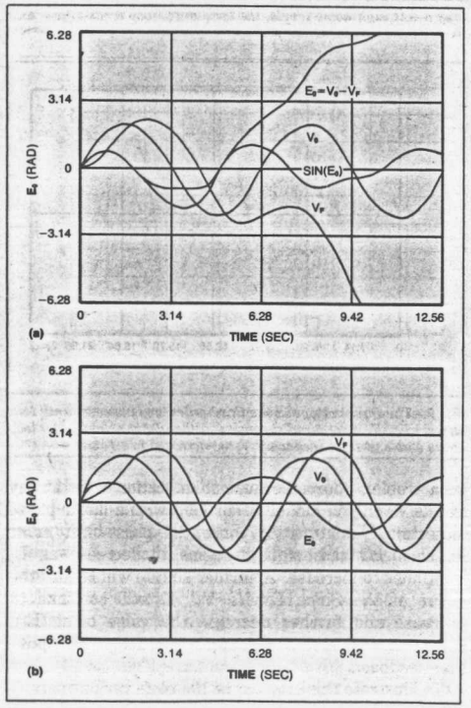


Fig 10—The feedback from the sine-wave detector is positive once E_e exceeds π/2 rad. As a result, E_e increases rather than decreases (a). Substituting a linear detector (b) for the sine-wave detector results in no evidence of instability.

that employs a linear detector.

For perfect error correction, V_F should be a mirror image of V_o. Unfortunately, phase and amplitude errors preclude this perfection. It appears that the amplitude error contribution from the sine-wave detector adds to the loop filter's phase error to cause the instabilities observed in these analyses. **EDN**

References

1. Rippy, Ron, "Basic programs solve differential equations quickly," *EDN*, February 6, 1986, pg 135.
2. Gardner, F M, *Phaselock Techniques*, 2nd ed, John Wiley & Sons, New York, NY, 1979.
3. Klapper, J, and J T Frankle, *Phase-Locked and Frequency-Feedback Systems*, Academic Press, New York, NY, 1972.

Author's biography

Ron Rippy is an electronics engineer with the Laboratory of Molecular Biophysics at the National Institute of Environmental Health Sciences in Research Triangle Park, NC. Ron designs and maintains nuclear magnetic resonance (NMR) spectrometers and has 22 years of experience in designing RF circuits and in programming computers. He enjoys programming a VAX computer at work and includes reading among his leisure activities.

Article Interest Quotient (Circle One)
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